DESIGNING RELIABLE HIGH-POWER LIMITER CIRCUITS WITH GaAs PIN DIODES

David G. Smith*, David D. Heston*, John Heston*, Brad Heimer*, and Ken Decker**

Raytheon Systems Company*, TriQuint Semiconductor**
13510 North Central Expressway
Dallas, Texas 75243

ABSTRACT — **This paper presents the latest GaAs PIN diode rf reliability data. An acceleration factor predicting lifetime as a function of diode perimeter and rf power level is proposed. Power handling measurements of an improved PIN diode layout that provides superior performance for both power handling and small signal loss / bandwidth is presented. Finally the design principles for a high power limiter will be reviewed.**

I. INTRODUCTION

Vertical GaAs PIN diodes have been available in MMIC circuits since their introduction in 1987 [1]. They have been used in limiter circuits [1,2,3], low-loss broadband switches [4], and attenuator circuits [2]. A new and improved diode layout has been made available by TriQuint Semiconductor. This paper reviews the new diode layout along with the improved small-signal performance and improved power handling capability it provides.

Very little data has been published on the reliability of GaAs PIN diodes and yet PIN diode circuits have been successfully used for approximately a decade in a number of different systems and applications. In the 1990 timeframe the small signal / dc reliability of GaAs PIN diodes were tested using a high temperature lifetest. The applied stress was a square wave (50% duty cycle) turning the diodes on and off to a 10mA current level. Greater than 6,000 hours of stress on 10 SPDT switch circuits at a temperature of 275°C were recorded with zero failures. In demonstration of this apparent robust reliability several thousand broadband switches have been fielded in a particular military system over the past ~10 years with many thousands of hours of operating life and no reported failures or system returns. This paper will examine the latest data available on GaAs PIN diode reliability. Two sets of reliability data have been taken: 1) rf burnout as a function of power level and diode perimeter and 2) dc bias reliability - median time to a 10% change in Ron of the PIN diode. The relationship between these two separate measurements is not fully established.

Understanding the reliability of PIN diodes under rf power levels as a function of diode size allows an optimum limiter circuit to be designed for a particular application. A cookbook approach to limiter design is included in this paper.

II. IMPROVED DIODE LAYOUT

TriQuint Semiconductor has recently introduced a new 'improved' PIN diode with an 'oval' shaped layout that provides enhanced performance for all types of PIN diode circuits [3,5]. Figure 1 compares the layout of a shunt PIN / NIP diode circuit using round diodes and the new oval diodes with equivalent perimeter. As the PIN diode is a vertical structure the words 'round' and 'oval' refer to the geometry of the mesa region. As published previously [6] the power handling capability of a GaAs PIN diode was measured to be proportional to its perimeter. However, insertion loss and bandwidth of a PIN diode circuit are a function of the parasitic capacitance of the diode, which is proportional to the diode's area. Figure 2 compares the area as a function of perimeter for round and oval shaped diodes.

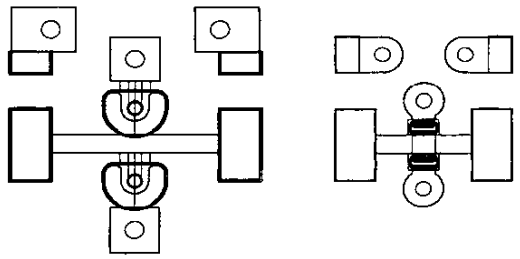

Fig. 1. Round vs. oval PIN / NIP test structures.

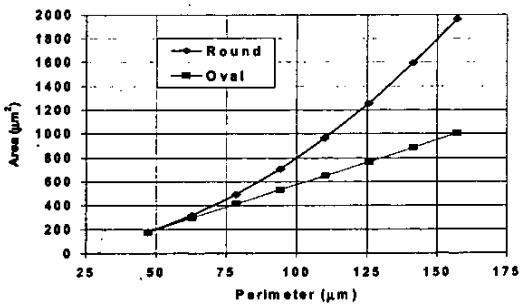

Fig. 2. Area vs. perimeter for round and oval PIN diodes.

By using an oval diode geometry, a greater than 50% reduction in area can be obtained for larger sized diodes when

0-7803-7239-5/02/$10.00 © 2002 IEEE

compared to a round diode of equivalent perimeter. This reduction in capacitance directly reduces the loss and increases the bandwidth of diode circuits.

Figure 3 shows measured rf burnout data on the new oval diodes along with data on round diodes. The burnout data shown in this figure is from the PIN / NIP test structures shown in Figure 1. As previously reported, 1 GHz is selected for these measurements to eliminate the impedance of the diodes as a factor in burnout. Additional details on this measurement are available in reference 6. Figure 4 shows the peak power handling of round and oval diodes as a function of perimeter. The data continues to show a relationship between power handling and perimeter.

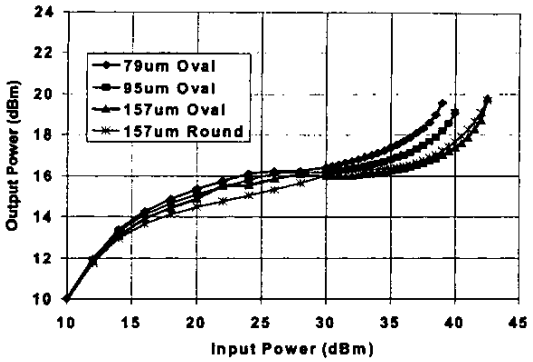

Fig. 3. Burnout curves for oval and round diodes.

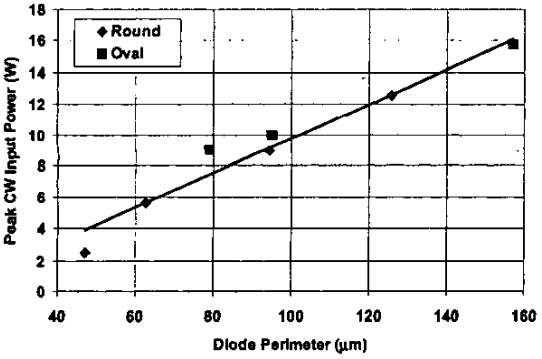

Fig. 4. Peak-power burnout vs. perimeter.

III. RF POWER HANDLING

With the peak burnout level of a GaAs PIN / NIP circuit established it is only natural to question how long this circuit would survive with reduced rf stress. A test examining the cw rf power handling of PIN diode limiters has been conducted at room temperature. Figure 5 shows the schematics for three X-band limiter circuits. The critical dimensions of the diodes have been included. Figure 6 shows the measured power handling capability at 7 to 8 GHz for the three circuits of Figure 5 as the rf power level is decreased from the levels established in Figure 4. A linear fit to all three data sets shows nearly parallel lines. An acceleration factor predicting time-to-failure as a function of rf

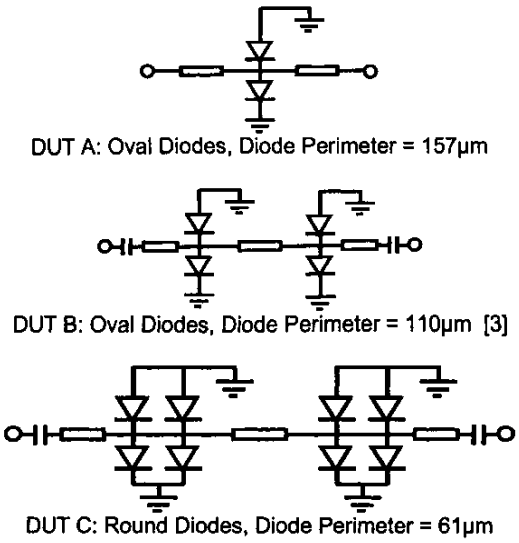

Fig. 5. Schematics for 3 limiter circuits.

power level is proposed by this data. A reduction of ~6 dB from the peak power level is required to achieve $1x10^6$ hours of lifetime under cw conditions at room temperature. For most system applications, the limiter functions as a protection circuit and is only turned on when exposed to high power levels. Based on the expected use of a limiter in a particular application, a different back-off level could be selected. The effects of temperature on the time-to-failure have not yet been measured.

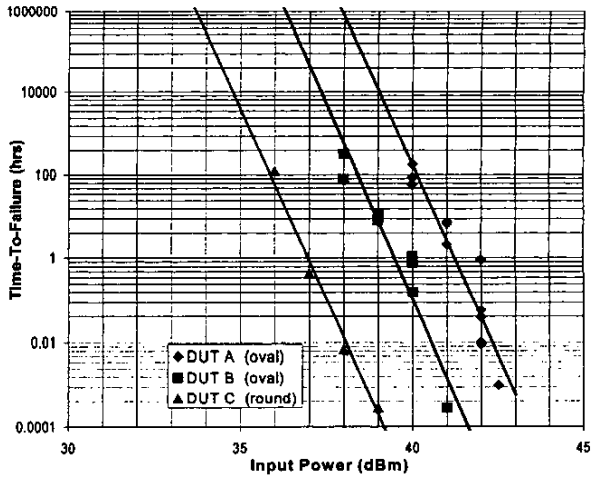

Fig. 6. Measured power handling for the limiter circuits of Figure 5.

IV. DC BIAS RELIABILITY

Although the initial dc lifetest conducted on PIN diodes in the ~1990 timeframe indicated extremely good reliability, it is possible that this test missed a small but very important degradation that was occurring in the PIN diode structure. As current passes through the PIN diode structure the 'on' resistance (Ron) of the PIN diode begins to change due to non-radiative recombination events at or in the vicinity of defects in the crystal structure. This change in Ron is a function of the current density in the PIN diode. Figure 7 shows the measured median time to 10% change in Ron as a function of the current density in the PIN diode at room temperature. There is a corresponding reduction in the carrier lifetime of the PIN diode.

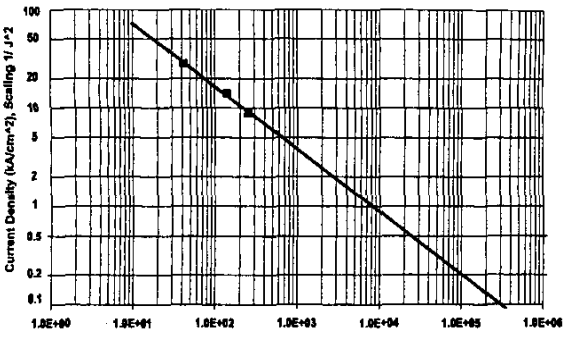

Fig. 7. Median time to 10% change in Ron.

The typical bias currents used in PIN diode circuits are relatively low. Using 5mA bias per diode in a standard switch or attenuator circuit shows that the time required to see a 10% change in Ron is ~2.5 years. Simulations show a barely perceptible change in the insertion loss (less than 0.1 dB change) of an attenuator or switch for increases in Ron as high as 30%.

III. BROADBAND HIGH-POWER LIMITER DESIGN – COOKBOOK

A common application of a limiter circuit is receiver protection in a transmit/receive (T/R) module. The limiter protects the receiver components from high-power signals through reflection of the incident signal. The diodes are turned on by high rf drive levels and provide a low impedance to ground, which reflects the incident signal. At low signal levels the insertion loss of a limiter is only a few tenths of a dB, but adds directly to the noise figure of the receiver, and therefore needs to be minimized. The major source of insertion loss in a limiter circuit is the off-state capacitance of the PIN diodes. A small amount of loss is also contributed by the matching elements.

A two-stage limiter can be designed to maximize limiting, power-handling capability and bandwidth. Figures 8 shows the schematic for a two-stage limiter. In this topology, at small-signal drive levels the diodes and transmission lines form a low-pass filter structure. The length and impedance of each transmission line supply a series inductance with the diodes providing parasitic shunt capacitance. By double stacking the input diodes, the shunt capacitance is reduced by a factor of 2. The advantages of stacking are most apparent when using larger size diodes.

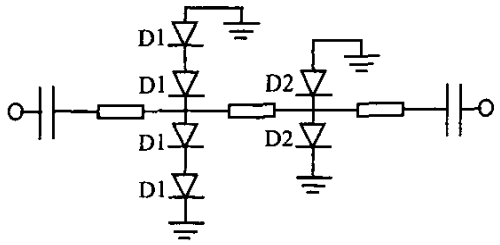

Fig. 8. Schematic for a two-stage limiter.

To optimize power handling, limiting and insertion loss of a limiter circuit, the design must start with the input section. The diode stack consists of 2 PIN and 2 NIP diodes in a shunt configuration. The diode size D1 should be selected to handle about 6 dB more than the peak power requirement. Then diode size D2 is chosen to equal the capacitance of the D1 stack. Finally, the inductance between D1 and D2 is chosen to complete the low pass filter design. If the peak power-handling requirement is extreme, a triple stack of D1 diodes may be required to achieve the desired bandwidth.

V. CONCLUSIONS

Data on dc and rf reliability and limiting characteristics of GaAs PIN diodes have been gathered to provide design information for high-power limiter circuits. Design techniques for optimizing the performance of a two-stage limiter have been reviewed.

REFERENCES

[1] D.J. Seymour, D.D. Heston, R.E. Lehmann, "Monolithic MBE GaAs PIN Diode Limiter," 1987 IEEE MTT-S Digest, pp. 35-37.

[2] D.J. Seymour, D.D. Heston, R.E. Lehmann, and D. Zych, "X-band Monolithic GaAs PIN Diode Variable Attenuation Limiter," 1990 IEEE MTT-S Digest, pp. 841-844.

[3] J. Carroll, "Performance Comparison of Single and Dual Stage MMIC Limiters," 2001 IEEE MTT-S Digest, pp. 841-844.

[4] D.D. Heston, D.J. Seymour, D. Zych, "100 MHz to 20 GHz Monolithic Single-pole, Two-, Three-, and Four-Throw GaAs PIN Diode Switches," 1991 IEEE MTT-S Digest, pp. 429-432.

[5] C. Rodenbeck, J.M. Carroll, R.A. Flynt, K.Chang, "Bias-Dependent Small-Signal Monolithic PIN Diode Modeling," Int. J. of RF/Microwave CAE, pp. 396-403,November 2001.

[6] D.G. Smith, D.D. Heston, D.L. Allen, "Designing High-Power Limiter Circuits with GaAs PIN Diodes," 1999 IEEE MTT-S Digest, pp. 329-332.